

**IN THE SPECIFICATION**

Please amend the paragraphs at page 2, line 16 to page 3, line 10, as follows:

A semiconductor integrated circuit device according to an aspect of the present invention includes:

unit cells each including a cell transistor and a ferroelectric capacitor connected between a source and a drain of the cell transistor;

memory cell blocks each including the unit cells connected in series between a first terminal and a second terminal and a block select transistor connected between the second terminal and a third terminal;

bit lines each of which connects commonly the third terminals of the memory cell blocks, the bit lines extending along a first direction;

sense amplifiers provided in correspondence to the bit lines and configured to amplify data supplied to the bit lines;

word lines each of which connects commonly gates of cell transistors in the memory cell blocks;

block select signal lines each of which connects commonly gates of block select transistors in the memory cell blocks;

plate lines each of which connects commonly the first terminals of the memory cell blocks, the plate lines extending along a second direction perpendicular to the first direction, and the memory cell blocks connected to one of the plate lines being connected to different ones of the sense amplifiers; and

a plate line driver to which a plurality of the plate lines are connected and which applies a potential to the plate lines.